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APPLICATION PAPERS

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FOR

STORAGE AND TRANSMISSION OF ONE-BIT DATA

ABSTRACT OF THE DISCLOSURE

Apparatus for storing or transmitting a one-bit digital signal comprises an input inverter for inverting a subset of the data bits of an input one-bit digital signal, to generate a bit-inverted signal; a storage or transmission medium for storing or transmitting the bit-inverted signal; and an output inverter for inverting the subset of the data bits of the bit-inverted signal, to regenerate the input one-bit digital signal.

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to the storage and transmission of one-bit (or "delta-sigma modulated) data, such as one-bit digital audio signals.

Description of the Prior Art

A convenient way of storing one-bit digital audio signals with currently available equipment is to multiplex groups of bits of the one-bit signal into data words, and then to record the data words on conventional multi-bit PCM recording equipment. For example, a one-bit signal at 64fs (where fs is, for example, 48 kHz) can be treated in this way by multiplexing 64 successive bits of the one-bit signal into 4 x 16-bit words, which can then be recorded on two stereo channels of a standard so-called AES/EBU digital audio recorder.

However, if there is a replay problem and the AES/EBU recorder mutes, its output goes to a continuous stream of digital zeroes. In a PCM system, a continuous stream of zeroes would be decoded as silence. However, in a one-bit data stream, a continuous stream of zeroes would be decoded as a very large magnitude audio signal -in fact, larger than the peak signal that most one-bit systems are designed to handle.

Similar problems can occur when one-bit data is stored or transmitted without necessarily reformatting the data into data words; if the signal disappears or mutes to a steady sequence of the same bit value, then this is equivalent to a very loud noise (or, more generally, a very large signal) in the one-bit system.

SUMMARY OF THE INVENTION

This invention provides apparatus for storing and/or transmitting a one-bit digital signal, the apparatus comprising:

an input inverter for inverting a subset of the data bits of an input one-bit digital signal, to generate a bit-inverted signal;

a storage and/or transmission medium for storing and/or transmitting the bit-inverted signal; and

an output inverter for inverting the subset of the data bits of the bit-inverted

signal, to regenerate the input one-bit digital signal.

The invention addresses the above problems by inverting a subset (e.g. 50%) of the data bits of the one-bit signal before they are recorded or transmitted, and then re-inverting that subset on reception or reproduction. This provides a processing scheme which is transparent to the signals when they are properly received or reproduced. However, if the signal disappears or the recording or transmission system outputs a continuous stream of ones or zeroes during a mute, the alternate bit inversion built into the replay or reception side of the apparatus will generate a one-bit output signal having a subset of inverted bits, representing a lower level signal in the one-bit domain. Indeed, in one embodiment, alternate bits of the input signal are inverted and so the output during a mute would be alternate ones and zeroes - the one-bit equivalent of digital silence.

This invention also provides apparatus for formatting a one-bit digital signal for storage and/or transmission, the apparatus comprising an inverter for inverting a subset of the data bits of an input one-bit digital signal, to generate a bit-inverted signal to be stored or transmitted.

This invention also provides apparatus for receiving a one-bit digital signal after storage and/or transmission, the apparatus comprising an inverter for inverting a subset of the data bits of the received one-bit digital signal.

This invention also provides a method of storing and/or transmitting a one-bit digital signal, the method comprising the successive steps of:

(i) inverting a subset of the data bits of an input one-bit digital signal, to generate a bit-inverted signal;

(ii) storing and/or transmitting the bit-inverted signal; and

(iii) inverting the subset of the data bits of the bit-inverted signal, to regenerate the input one-bit digital signal.

The above, and other objects, features and advantages of this invention will be apparent from the following detailed description of illustrative embodiments which is to be read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 schematically illustrates a data recording system; and

Figure 2 schematically illustrates a bit inverter.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the drawings, a one-bit digital data recording system comprises a demultiplexer 10 for receiving an input one-bit digital audio signal 20, a data recorder 30 (in this case, a so-called AES/EBU standard digital audio recorder), and a multiplexer 40 for generating an output one-bit digital audio signal 50. Bit-inverters 60 and 70 are connected between the demultiplexer 10 and the data recorder 30 and between the data recorder 30 and the multiplexer 40.

The input one-bit signal 20 comprises successive individual data bits:

$$b_1, b_2, b_3, b_4, b_5, b_6, b_7, \ldots, \ldots b_{63}, b_{64}, b_{65}, b_{66}, \ldots$$

However, the AES/EBU recorder 30 is designed to record 16-bit data words (each representing a PCM audio sample) at a sampling rate of 48kHz.

So, the demultiplexer 10 forms groups of the data bits of the one-bit input signal and passing them to the AES/EBU recorder 30 for recording as though they were 16-bit PCM data words.

In the present example, the one-bit digital audio signal has a data rate (bit rate) of 64fs, where fs is 48kHz, and so for each sample period of the 48kHz AES/EBU recorder, 64 bits of the one-bit digital audio signal must be multiplexed and recorded as data words. Therefore, four 16-bit data words are required to be formed for each 48kHz sample period.

Four data words per sample period correspond to four audio channels being recorded on the AES/EBU data recorder. In fact, this can be configured as two stereo channels to accommodate the four data words per sample period. The two stereo channels are represented by pairs of signals 80, 90 (not shown) in Figure 1[1].

The way in which the demultiplexer 10 divides the input one-bit digital audio signal into the data words is first to generate two bit streams, each comprising alternate data bits from the input one-bit signal. Therefore, the bit streams would

[1] In fact, a stereo pair in a PCM AES/EBU system comprises alternate PCM samples, and so each stereo pair would be carried by a single schematic "wire" in Figure 1. However, to assist in the explanation, four "wires" are shown emerging from the demultiplexer 10.

contain:

bit stream 1: $b_1, b_3, b_5, b_7, \ldots$

bit stream 2: $b_2, b_4, b_6, b_8, \ldots$

Each of the two bit streams is then sub-divided to form the two channels of a respective stereo pair, for recording on the AES/EBU recorder. This is done by taking alternate groups of 16 adjacent bits and assigning them to one of the left and right channels of that stereo pair. So, using the notation established above, the following 16-bit data words would be generated for recording on the AES/EBU recorder 30:

Stereo pair A:

left: $b_1, b_3, b_5 \ldots b_{29}, b_{31}$

right: $b_{33}, b_{35}, b_{37}, b_{39} \ldots b_{61}, b_{63}$

Stereo pair B:

left: $b_2, b_4, b_6 \ldots b_{30}, b_{32}$

right: $b_{34}, b_{36}, b_{38}, b_{40} \ldots b_{62}, b_{64}$

The inverters 60 invert the data bits of one of the stereo pairs before recording. Similar inverters 70 invert the same stereo pair when it is reproduced from the recorder 30. Because each stereo pair is formed from a respective bit stream, which in turn is formed of alternate bits of the input one-bit signal, the inverters 60 have the effect of inverting alternate bits of the input one-bit signal. These bits are then re-inverted on replay by the inverters 70 to reconstruct the bits of the input one-bit signal.

The multiplexer 40 operates in a complementary manner to the demultiplexer 10, to convert replayed 16-bit data words into the one-bit signal $b_1, b_2, b_3, b_4 \ldots$

One advantage of this embodiment is that if there is an error which leads to a failure during replay on the AES/EBU recorder 30, that recorder will "mute" to a

signal comprising successive digital zeroes. This is no problem in a PCM system, because a signal of all zeroes represents silence. However, in a one-bit signal, a signal of all zeroes represents a very loud noise indeed.

However, since the inverters 70 are operable to invert alternate bits output by the AES/EBU recorder (alternate in the sense that they become alternate within the one-bit signal output by the multiplexer 40), a mute signal is transformed into an output one-bit signal comprising alternate ones and zeroes. A signal of alternate ones and zeroes is a close representation of silence in a one-bit system.

Similarly, when replay is ceased (e.g. by pressing the stop button on the recorder 30) a mute signal may also be output and will be treated in the same way.

In other embodiments, the recorder 30 may be replaced by a transmission medium such as a cable, optical fibre or satellite link. If the transmission medium is disconnected or fails in any other way, or if it mutes through any transmission problems, then the inverters 70 have the same effect of transforming a PCM digital silence into a one-bit digital silence signal.

It is not of course necessary for the digital silence signal in the one-bit system to be alternate ones and zeroes (and of course it is not necessary for the signal to be multiplexed into data words for the inversion to take place). In fact, any inversion pattern which results in a silence signal having a substantially even distribution of ones and zeroes could perform the same function, and indeed there can be advantages in using an inversion pattern which inverts, perhaps, four bits at "random" positions within each 8-bit group of the input one-bit signal, to "spread out" the spectral energy of the "digital silence" signal. (Here, it is noted that a concentration of spectral energy within a one-bit digital signal can lead to instability of signal processing apparatus receiving that signal.)

Figure 2 schematically illustrates a generic bit inverter which could perform this function in place of the inverters 60 and 70.

In Figure 2, a bit stream to be inverted is supplied on an input 100, and a bit-inverted bit stream is generated at an output 110.

The inversion is performed by an exclusive-OR gate 120, which acts on two inputs: the input signal 100 and a bit stream generated by a shift register 130 connected in a feedback arrangement so that it repeatedly supplies a sequence of (in

this case) eight bits to the exclusive-OR gate 120.

When the shift register 130 supplies a 0 to the exclusive-OR gate 120, no inversion takes place. When the shift register 130 supplies a 1 to the exclusive-OR gate 120, the current input bit on the input 100 is inverted.

Although illustrative embodiments of the invention have been described in detail herein with reference to the accompanying drawings, it is to be understood that the invention is not limited to those precise embodiments, and that various changes and modifications can be effected therein by one skilled in the art without departing from the scope and spirit of the invention as defined by the appended claims.